Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1 – 20 (canceled).

21 (currently amended). A method for reducing impedance within a reference path in a printed circuit board comprising the steps of:

forming said printed circuit board comprising a plurality of conductive layers, wherein one of said plurality of conductive layers is a first layer, wherein one of said plurality of conductive layers is a second layer, wherein said printed circuit board further comprises two or more vias interconnecting two or more conductive layers of said plurality of conductive layers, wherein a first of said two or more vias is part of a signal path configured to carry said signal from said first layer to said second layer, wherein a second of said two or more vias is part of a reference path configured to carry said signal from a third layer to a fourth conductive layer; and

embedding an electrical component in said second of said two or more vias between two conductive layers of said plurality of conductive layers.

22 (original). The method as recited in claim 21, wherein said electrical component is a capacitor.

23 (original). The method as recited in claim 21, wherein said second via of said two or more vias is a via adjacent to said first via of said two or more vias.

24 (original). The method as recited in claim 21, wherein said electrical component has a cylindrical configuration.

25 (original). The method as recited in claim 21, wherein a diameter from one end of said electrical component changes to an other end of said electrical component, wherein said second via of said two or more vias is configured so that one end of said second via of said two or more vias changes in diameter to an other end of said second via of said two or more vias.

26 (original). The method as recited in claim 25 further comprising the step of:

embedding said electrical component between two conductive layers of said plurality of conductive layers within said printed circuit board by adjusting the diameter of said electrical component and the diameter of said second via of said two or more vias.

27 (currently amended). ~~The method as recited in claim 21,~~ A method for reducing impedance within a reference path in a printed circuit board comprising the steps of:

forming said printed circuit board comprising a plurality of conductive layers, wherein one of said plurality of conductive layers is a first layer, wherein one of said plurality of conductive layers is a second layer, wherein said printed circuit board further comprises two or more vias interconnecting two or more conductive layers of said plurality of conductive layers, wherein a first of said two or more vias is part of a signal path configured to carry said signal from said first layer to said second layer, wherein a second of said two or more vias is part of a reference path configured to carry said signal from a third layer to a fourth conductive layer; and

embedding an electrical component in said second of said two or more vias between two conductive layers of said plurality of conductive layers;

wherein said electrical component has a greater diameter in a center than at ends of said electrical component, wherein each end of said electrical component has a conductive cap which is tinned.

28 (original). The method as recited in claim 21, wherein said electrical component is packaged as a pin, wherein each end of said electrical component is soldered to said two conductive layers of said plurality of conductive layers within said printed circuit board.

29 (original). The method as recited in claim 21, wherein said second layer is configured to carry said signal to a load, wherein said third layer is configured to return said signal from said load.

30-40 (canceled).

41 (new). A method for reducing impedance of a transmission line in a multi-layer printed circuit board, comprising:

forming said printed circuit board, wherein said circuit board includes first, second, third, and fourth conductive layers, wherein the first and second layers form a signal path of the transmission line and wherein the third and fourth layers form a reference path of the transmission line;

forming a first via connecting said first layer to said second layer; and

forming a second via connecting said third layer to said fourth layer, wherein said forming of said second via includes embedding a capacitor in the via between the third layer and the fourth layer.

42 (new). The method of claim 41, wherein the first layer is a top layer of the printed circuit board and the second layer is a bottom layer, and further wherein the third layer is adjacent the first layer and the fourth layer is adjacent the second layer.